

1.(Canceled). A semiconductor structure comprising:

a substrate having a major surface;

5 at least one trench formed in said substrate extending from said major surface, said trench includes inner surfaces filled with conductive material which is electrically separated from said substrate by insulating material;

10 a first Insulating layer disposed on said major surface above said trench, said first insulating layer having a first contact opening;

15 a first conductive layer disposed above said first insulating layer and in contact with said conductive material in said trench through said first contact opening, said first conductive layer having a conductivity higher than the conductivity of said conductive material;

20 a second insulating layer disposed above said first conductive layer, said second insulating layer having a second contact opening; and

25 a second conductive layer disposed above said second insulating layer and in contact with said substrate through said second contact opening.

2. (Canceled) The semiconductor structure as set forth in claim 1 further including a source layer disposed in said substrate extending from said major surface.

30 3 (Canceled). The semiconductor structure as set forth in claim 2 wherein said structure is a MOSFET structure having a source, a drain and a gate, said source includes said source layer, said drain includes said substrate, and said gate includes said trench.

35 4 (Canceled). The semiconductor structure as set forth in claim 1 wherein said second conductive layer comprises a substantially rectangular shape disposed on said major surface of said substrate, wherein said rectangular shape of said second conductive layer having no elongated voids extended therein.

40 5 (Canceled). The semiconductor structure as set forth in claim 1 wherein said first insulating layer comprises silicon dioxide and said second insulating layer comprises borophosphorous silicon glass.

- 5 6 (Canceled). The semiconductor structure as set forth in claim I wherein said first and second insulating layers are made of material selected from a group consisting of silicon dioxide, borophosphorous silicon glass, and phosphorous silicon glass.
- 7 (Canceled). The semiconductor structure as set forth in claim I wherein said conductive material inside said trench comprises polycrystalline silicon.
- 10 8 (Canceled). The semiconductor structure as set forth in claim I wherein said first and second conductive layers comprise metal.
- 15 9 (Canceled). The semiconductor structure as set forth in claim 8 wherein said metal comprises aluminum.
- 20 10 (Canceled). The semiconductor structure as set forth in claim I wherein said first and second conductive layers are made of material selected from a group consisting of copper, aluminum, aluminum suicide, and alloy of aluminum, silicon and copper.
- 25 11 (Canceled). The semiconductor structure as set forth in claim I wherein said second conductive layer is plated with a metal layer.
- 30 12 (Canceled). The semiconductor structure as set forth in claim II wherein said metal layer comprises copper.
- 35 13 (Canceled). The semiconductor structure as set forth in claim I wherein said trench is a low-resistance trench, said semiconductor structure includes a plurality of said low-resistance trenches, said semiconductor structure further comprising a plurality of low-capacitance trenches disposed in said substrate, each of said low-capacitance trenches being disposed without said first conductive layer disposed thereabove and having a trench width substantially narrower than the corresponding trench width of said low-resistance trench, said low-resistance trenches and said low-capacitance trenches being disposed interleaving with each other in said substrate.
- 40 14 (Canceled). The semiconductor structure as set forth in claim I wherein said trench is elongated in shape.

15 (Canceled). A semiconductor structure comprising:

a substrate having a major surface;

5 a plurality of trenches formed in said substrate extending from said major surface, some of said trenches being orientated in a first direction and others of said trenches being orientated in a second direction, each of said trenches being filled with
10 conductive material which is electrically separated from said substrate by insulating material;

an insulating layer disposed on said major surface above said trenches, said insulating layer having a plurality of contact
15 openings positioned above said trenches along said first and second directions; and

a conductive layer disposed above said insulating layer and in contact with said conductive material in said trenches through
20 said contact openings said conductive layer having conductivity higher than the conductivity of said conductive material.

25 16 (Canceled). The semiconductor structure as set forth in claim 15 wherein said conductive layer includes crisscrossing segments disposed above said major surface of said substrate, some of said segments being orientated in said first direction and others of said segments being orientated in said second direction, each of said segments being disposed in substantial alignment with one of said
30 trenches.

17 (Canceled). The semiconductor structure as set forth in claim 16 further including a source layer disposed in said substrate extending from said major surface.

35 18 (Canceled). The semiconductor structure as set forth in claim 17 wherein said structure is a MOSFET structure having a source, drain and a gate, said source includes said source layer, said drain includes said substrate, and said gate includes said trenches.

40 19 (Canceled). The semiconductor structure as set forth in claim 15 wherein said conductive material inside said trench comprises polycrystalline silicon.

20 (canceled).

21 (Canceled). The semiconductor structure as set forth in claim 15 wherein said insulating layer is a first insulating layer, said contact openings are first contact openings and said conductive layer is a first conductive layer, said structure further comprising:

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a second insulating layer disposed above said first conductive layer, said second insulating layer having a plurality of second contact openings; and

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a second conductive layer disposed above said second insulating layer and in contact with said substrate through said second contact openings.

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22 (Canceled). The semiconductor structure as set forth in claim 21 wherein said second conductive layer is plated with a metal layer.

23 (Canceled). The semiconductor structure as set forth in claim 22 wherein said metal layer comprises copper.

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24 (Canceled). The semiconductor structure as set forth in claim 21 wherein said second conductive layer being substantially rectangular in shape disposed on said major surface of said substrate, wherein said rectangular shape of said second conductive layer having no elongated voids extended therein.

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25 (Canceled). The semiconductor structure as set forth in claim 24 wherein:

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said first and second insulating layers are made of material selected from a group consisting of silicon dioxide, borophosphorous silicon glass, and phosphorous silicon glass.

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26 (Canceled). The semiconductor structure as set forth in claim 21 wherein said first and second conductive layers are made of material selected from a group consisting of copper, aluminum, aluminum silicide, and alloy of aluminum, silicon and copper.

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27 (Canceled). A semiconductor structure comprising:

a substrate having a major surface;
a plurality of trenches formed in said substrate extending from said major surface, some of said trenches being orientated in a first direction and others of said trenches being orientated in a second direction, each of said trenches being filled with
conductive material which is electrically separated from said

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- 5 substrate by insulating material;
a first insulating layer disposed on said major surface above
said trenches, said first insulating layer having a plurality of
first contact openings above said trenches along said first and
second directions;
a first conductive layer having crisscrossing segments
disposed above said major surface of said substrate, some of
said segments being orientated in said first direction and
others of said segments being orientated in said second
10 direction, each of said segments being disposed in substantial
alignment and in contact with one of said trenches through
one of said first openings, said first conductive layer having
conductivity higher than the conductivity of said conductive
material;
15 a second insulating layer disposed above said first conductive
layer, said second insulating layer having a plurality of second
contact openings; and
a second conductive layer disposed above said second
insulating layer and in contact with said substrate through
20 said second contact openings.
- 25 28 (Canceled). The semiconductor structure as set forth in claim 27
further including a source layer disposed in said substrate extending
from said major surface, wherein said structure is a MOSFET
structure having a source, a drain and a gate, said source includes
said source layer, said drain includes said substrate, and said gate
includes said trenches.
- 30 29 (Canceled). The semiconductor structure as set forth in claim 28
wherein said first insulating layer comprises silicon dioxide, said
second insulating layer comprises borophosphorous silicon glass,
said conductive material inside said trench comprises polycrystalline
silicon, and said first and second conductive layers comprise metal.
- 35 30 (Canceled). The semiconductor structure as set forth in claim 29
wherein said second conductive layer being substantially
rectangular in shape disposed on said major surface of said
substrate, wherein said rectangular shape of said second conductive
layer having no elongated voids extended therein, thereby allowing
40 bonding wires to be substantially unrestrictively attached onto said
second conductive layer.
- 31 (Canceled). The semiconductor structure as set forth in claim 30
wherein said second conductive layer is plated with copper.

32 (Previously Presented). A semiconductor structure comprising:
a substrate having a major surface;
a plurality of low-resistance trenches formed in said substrate
extending from said major surface, some of said low-resistance
5 trenches being orientated in a first direction and others of said
low-resistance trenches being orientated in a second direction,
each of said low-resistance trenches being filled with
conductive material which is electrically separated from said
substrate by insulating material. said conductive material
10 comprises polycrystalline silicon;
a first insulating layer disposed on said major surface above
said low-resistance trenches, said first insulating layer having a
plurality of first contact openings above said low-resistance
trenches along said first and second directions, said first
15 insulating layer comprises silicon dioxide;
a first conductive layer having crisscrossing segments disposed
above said major surface of said substrate, some of said
segments being orientated in said first direction and others of
said segments being orientated in said second direction. each of
20 said segments being disposed in substantial alignment and in
contact with one of said low-resistance trenches through one of
said first openings;
a plurality of low-capacitance trenches disposed in said
substrate, each of said low-capacitance trenches being disposed
25 without said first conductive layer disposed thereabove and
having a trench width substantially narrower than the
corresponding trench width of each of said low-resistance
trenches, said low-resistance trenches and said low-capacitance
trenches being disposed interposing with each other in said
30 substrates;
a second insulating layer disclosed above said first conductive
layer, said second insulating layer having a plurality of second
contact openings, said second insulating layer comprises
borophosphorous silicon glass;
35 a second conductive layer disposed above said second
insulating layer and in contact with said substrate through said
second contact openings, said second conductive layer being
substantially rectangular in shape disposed on said major
surface of said substrate, wherein said rectangular shape of
40 said second conductive layer having no elongated voids
extended therein, thereby allowing bonding wires to be
substantially unrestrictively attached onto said second
conductive layer, said second conductive layer is plated with
copper; and

5 a source layer disposed in said substrate extending from said major surface, wherein said structure is a MOSFET structure having a source, a drain and a gate, said source includes said source layer. said drain includes said substrate, and said gate includes said low-resistance and low-capacitance trenches.

33 (Previously Presented). A semiconductor structure comprising:

- 10 a substrate having a major surface;
- 15 a plurality of low-resistance trenches disposed in said substrate extending from said major surface, some of said low-resistance trenches being orientated in a first direction and others of said low-resistance trenches being orientated in a second direction, each of said low-resistance trenches being filled with conductive material which is electrically separated from said substrate by insulating material;
- 20 an insulating layer disposed on said major surface above said trenches, said insulating layer having a plurality of contact openings positioned above said trenches along said first and second directions;
- 25 a conductive layer disposed above said insulating layer and in contact with said conductive material in said trenches through said contact openings; and
- 30 a plurality of low-capacitance trenches disposed in said substrate, each of said low-capacitance trenches being formed without said conductive layer disposed thereabove and having a trench width substantially narrower than the corresponding trench width of each of said low-resistance trenches, said low-resistance trenches and said low-capacitance trenches being disposed interleaving with each other in said substrate.
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